PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference NANY/20500250/JW/mt	FOR FURTHER ACTION	See Form PCT/IPEA/416
International application No. PCT/SG2005/000043	International filing date *(day/month/year)* 17 February 2005	Priority date *(day/month/year)* 17 February 2004

International Patent Classification (IPC) or national classification and IPC

Int. Cl.

H01L 27/146 (2006.01) ***G01J 3/46*** (2006.01)

Applicant

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1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 3 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. [X] *(sent to the applicant and to the International Bureau)* a total of 7 sheets, as follows:
      - [X] sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
      - [ ] sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.

   b. [ ] *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing and/or table related thereto, in electronic form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).
4. This report contains indications relating to the following items:

[X]	Box No. I	Basis of the report
[ ]	Box No. II	Priority
[ ]	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
[ ]	Box No. IV	Lack of unity of invention
[X]	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
[ ]	Box No. VI	Certain documents cited
[ ]	Box No. VII	Certain defects in the international application
[ ]	Box No. VIII	Certain observations on the international application

Date of submission of the demand	Date of completion of this report
7 December 2005	09 January 2006
Name and mailing address of the IPEA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. (02) 6285 3929	Authorized Officer S. T. PRING Telephone No. (02) 6283 2210

Box No. I Basis of the report

1. With regard to the **language**, this report is based on:

[X] The international application in the language in which it was filed

[ ] A translation of the international application into , which is the language of a translation furnished for the purposes of:

[ ] international search (under Rules 12.3(a) and 23.1 (b))

[ ] publication of the international application (under Rule 12.4(a))

[ ] international preliminary examination (Rules 55.2(a) and/or 55.3(a))

2. With regard to the **elements** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

[ ] the international application as originally filed/furnished

[X] the description:

pages **1-30** as originally filed/furnished
pages* received by this Authority on with the letter of
pages* received by this Authority on with the letter of

[X] the claims:

pages as originally filed/furnished
pages* as amended (together with any statement) under Article 19
pages* **31-37** received by this Authority on **14 December 2005** with the letter of 2 December 2005
pages* received by this Authority on with the letter of

[X] the drawings:

pages **1/20-20/20** as originally filed/furnished
pages* received by this Authority on with the letter of
pages* received by this Authority on with the letter of

[ ] a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing.

3. [ ] The amendments have resulted in the cancellation of:

[ ] the description, pages
[ ] the claims, Nos.
[ ] the drawings, sheets/figs
[ ] the sequence listing *(specify)*:
[ ] any table(s) related to the sequence listing *(specify)*:

4. [ ] This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).

[ ] the description, pages
[ ] the claims, Nos.
[ ] the drawings, sheets/figs
[ ] the sequence listing *(specify)*:
[ ] any table(s) related to the sequence listing *(specify)*:

* *If item 4 applies, some or all of those sheets may be marked "superseded."*

International application No.
PCT/SG2005/000043

Box No. V **Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	1-41	YES
	Claims		NO
Inventive step (IS)	Claims	1-41	YES
	Claims		NO
Industrial applicability (IA)	Claims	1-41	YES
	Claims		NO

2. Citations and explanations (Rule 70.7)

Novelty and Inventive Step

EP 1 006 585 discloses a three colour detection pixel sensor comprising a top doped p+ layer contacted by an N-well beneath, and P-substrate beneath that in turn. Electrical gate contacts on the top surface contact both sides of the p+ region and the N-well and P- substrate in turn to allow current to flow when each layer detects a certain colour wavelength.

US 5 965 875 discloses a three colour sensor with three stacked n-p-n- levels with a possible fourth doped p region below again. Electrical contacts are placed in contact with the regions to determine current flowing due to impinging light.

SU 1689768 discloses a three pn junction colorimetric sensor one above another which use photocurrents induced by a particular wavelength in each level.

JP 07-038136 discloses a photodetective element composed of pn junctions different to each other in wavelength selectivity to induce a current proportional to the light detected.

None of the cited art discloses two junctions with a connecting material between the junctions. Therefore claims 1-41 can be said to be novel and to have an inventive step.

The claims are directed to manufacturing and therefore can be said to Industrially applicable.

WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a substrate having a surface,

a first *pn*-junction defining a first depletion region formed on said substrate at a first depth relative to said surface,

a second *pn*-junction defining a second depletion region formed on said substrate at a second depth relative to said surface deeper than said first depth,

a doped, photo-conductive channel formed on said substrate between said first and second *pn*-junctions,

said first and second depths chosen to generate (i) charge carriers in said first depletion region in response to light of a first wavelength band incident on said surface, (ii) charge carriers in said second depletion region in response to light of a second wavelength band incident on said surface, and (iii) charge carriers in said channel in response to light of a third wavelength band incident on said surface,

doped drain and source regions on said substrate in communication with said channel;

first and second electrical interconnects in communication with said source and drain regions, respectively; and

third and fourth electrical interconnects in communication with said first and second *pn*-junctions, respectively;

whereby incident light on said surface at said first, second, and third wavelength bands are detectable through currents through said first, second, third and fourth electrical contacts.

2. The semiconductor device of claim 1, wherein said first depth is between 0.02 to 0.5 microns and said second depth is between 2 and 10 microns.

3. The semiconductor device of claim 1 or claim 2, wherein said substrate comprises a semiconductor wafer, said channel is epitaxially grown on said wafer.

4. The semiconductor device of any one of claims 1 to 3, wherein said electrical interconnects and said surface are on a same side of said substrate.

5. The semiconductor device of any one of claims 1 to 3, wherein said first, second and third electrical interconnects and said surface are on a same side of said substrate, and said fourth electrical interconnect is on an opposite side of said substrate.

6. The semiconductor device of any one of claims 1 to 5, comprising a top gate region adjoining said channel forming said first *pn*-junction and a bottom gate region adjoining said channel forming said second *pn*-junction, said channel doped of a first conductive type, said gate regions doped of an opposite, second conductive type, thus forming a junction field-effect transistor (JFET) on said substrate.

7. The semiconductor device of claim 6, wherein said first conductive type is *n*-type, said channel having a doping concentration from about 1E14 to about 1E16 cm^{-3}, said top gate region having a doping concentration from about 1E16 to about 1E19 cm^{-3}, and said bottom gate region having a doping concentration from about 1E14 to about 1E19 cm^{-3}.

8. The semiconductor device of claim 7, wherein at least one of said source and drain regions is of said first conductive type and has a doping concentration of about 1E20 cm^{-3}.

9. The semiconductor device of claim 8, further comprising a contact region formed on said substrate connecting said bottom gate region to said fourth electrical interconnect, said contact region being of said second conductive type at a concentration of at least 1E19 cm^{-3}.

10. The semiconductor device of any one of claims 6 to 9, further comprising a top region of said first conductive type formed on said substrate between said surface and said top gate region, thus forming a third *pn*-junction defining a third depletion region at a third depth relative to said surface, and an electrical interconnect in communication with said third depletion region for detecting a current therefrom.

11. The semiconductor device of any one of claims 6 to 9, further comprising an additional top gate region of said second conductive type formed on said substrate adjoining said channel, thus forming a third *pn*-junction defining a third depletion region, and an electrical interconnect in communication with said third depletion region for detecting a current therefrom.

12. The semiconductor device of claim 11, wherein said top gate regions have different doping concentrations.

13. The semiconductor device of claim 11, wherein said third *pn*-junction is at a depth relative to said surface less than said first depth.

14. The semiconductor device of any one of claims 6 to 13, wherein said channel comprises a buried region adjoining said bottom gate region forming said second *pn*-junction, said buried region having a doping concentration higher than that of said bottom gate region so that said second depletion region mainly develops within said bottom gate region.

15. The semiconductor device of any one of claims 6 to 14, wherein said top gate region comprises a central region and a protective ring region around a periphery of said central region, said protective ring region having a higher doping concentration and being thicker than said central region.

16. The semiconductor device of any one of claims 6 to 15, wherein said JFET is a first FET, and further comprising a second FET having a source, a drain, a channel of said second conductive type, and a gate of said first conductive type, said source region of said first FET connected to said source of said second FET, said drain region of said first FET being connected to said gate of said second FET, said drain of said second FET being connected to a gate region of said first FET, thus forming a dual-FET device.

17. The semiconductor device of claim 16, wherein said FET is a JFET or a depletion-metal-oxide semiconductor FET (d-MOSFET).

18. The semiconductor device of any one of claims 6 to 17, further comprising (i) one or more regions of alternating conductive types formed on said substrate extending from said bottom gate region away from said surface, thus forming one or more additional *pn*-junctions at different depths relative to said surface and forming one or more additional channels each between two adjacent *pn*-junctions; (ii) additional doped drain and source regions on said substrate in communication with each one of said one or more additional channels, respectively; and (iii) additional electrical interconnects in communication with said additional one or more *pn*-junctions and said one or more channels, wherein said different depths are chosen to generate charge carriers in response to light of different wavelength bands incident on said surface respectively in said one or more regions, whereby incident light on said surface of said different wavelength bands are detectable through said additional source and drain regions, and said additional electrical interconnects.

19. A semiconductor device, comprising

a substrate having a surface;

a doped, photo-conductive channel of a first conductive type formed on said substrate beneath said surface, said channel having a bottom at a first depth relative to said surface,

doped drain and source regions formed on said substrate beneath said surface in communication with said channel, said source region having a bottom at a second depth relative to said surface, said drain region having a bottom at a third depth relative to said surface;

a doped gate region of an opposite, second conductive type formed on said substrate beneath and adjoining said channel and said source and drain regions, thus forming a *pn*-junction defining a depletion region;

said first depth chosen to generate charge carriers in said channel in response to light of a first wavelength band incident on said surface,

said second depth chosen to generate charge carriers in said depletion region proximate said bottom of said source region in response to light of a second wavelength band incident on said surface;

said third depth chosen to generate charge carriers in said depletion region proximate said bottom of said drain region in response to light of a third wavelength band incident on said surface;

first and second electrical interconnects in communication with said source and drain regions, respectively;

a third electrical interconnect in communication with said *pn*-junction;

whereby incident light on said surface at said first, second, and third wavelength bands are detectable through currents through said first, second, and third electrical interconnects.

20. The semiconductor device of claim 19, wherein said first depth is from 0.05 to 0.5 microns, said second depth is from 0.3 to 2 microns and said third depth is from 2 to 10 microns.

21. The semiconductor device of claim 19 or claim 20, wherein said first conductive type is *n*-type, said channel has a doping concentration of from about 1E15 to about 1E19 cm^{-3}, said source and drain regions having a doping concentration of about 1E20 cm^{-3}, and said gate region having a doping concentration from about 1E14 to about 1E15 cm^{-3}.

22. The semiconductor device of any one of claims 19 to 21, further comprising one or more contact regions of said first conductive type formed within said channel distributed between said drain and source regions, said one or more contact regions having a higher doping concentration than said channel, and an electrical interconnect in contact with each one of said one or more contact regions for detecting an output signal therefrom.

23. The semiconductor device of any one of claims 19 to 21, wherein a sub-region in said gate region adjoining said channel comprises a buried layer having a higher doping concentration than said channel so as to limit extension of said depletion region into said gate region.

24. The semiconductor device of any one of claims 19 to 21, further comprising an oxide layer in contact with said channel and said drain region, a metal layer formed on said oxide layer thus forming a metal-oxide-semiconductor (MOS) gate, and an electrical interconnect in communication with said metal layer for detecting a current therefrom.

25. The semiconductor device of claim 19, further comprising an additional doped channel beneath said gate region and an additional doped gate region beneath said additional channel, doped source and drain regions in communication with said additional channel and an electrical interconnect in communication with said additional gate region for detecting currents therefrom respectively.

26. The semiconductor device of claim 25, further comprising source and drain regions in communication with said gate region between said channels for detecting a current between said source and drain regions through said gate region.

27. The semiconductor device of any one of claims 1 to 26, wherein said substrate is made substantially of silicon or a silicon-based substance.

28. A photo-sensing device comprising a plurality of photo-sensing units, each unit being a semiconductor device of any one of claims 1 to 27.

29. The photo-sensing device of claim 28, wherein two or more of said plurality of photo-sensing units share either a common source region or a common gate region, or both.

30. The photo-sensing device of claim 28 or claim 29, wherein said plurality of photo-sensing units form a pattern for imaging.

31. The photo-sensing device of any one of claims 28 to 30, wherein two or more of said photo-sensing units are stacked one below another.

32. A method of photo-sensing comprising:

biasing a junction field effect transistor (JFET) to generate

a conducting channel between a source and a drain of said JFET, said conducting channel having an absorption section below a light-transmitting surface of said JFET, said absorption section having a pre-determined photo-conductivity spectral response, and

at least two depleted regions below said light-transmitting surface, each having a photo-electric spectral response peaking at a distinct, pre-determined wavelength;

illuminating said light-transmitting surface with light;

sensing an output signal derived from said channel indicative of the intensity of light absorbed therein; and

for each particular one of said depleted regions, sensing an output signal derived from said particular depleted region indicative of the intensity of light absorbed therein.

33. The method of claim 32, wherein said one or more depleted regions comprise two depleted regions at different depths below said light-transmitting surface.

34. The method of claim 32 or claim 33, wherein said sensing an output signal comprises sensing a current.

35. The method of claim 34, wherein said sensing an output signal comprises sensing a drain-source current from said drain to said source through said conducting channel, and said sensing an output signal derived from said particular depleted region comprises sensing a gate current from a gate in contact with said particular depleted region.

36. The method of claim 35, wherein said sensing a drain-source current comprises:

sensing a drain-source photo-induced current variation based on: sensing a drain current from said drain during said illuminating, obtaining a quiescent drain-source current, and calculating said photo-induced drain-source current variation by subtracting from said drain current said quiescent drain-source current and the sum of said gate currents,

37. The method of claim 36, wherein said obtaining a quiescent drain-source current comprises sensing a quiescent source current from said source and a quiescent drain current from said drain without illuminating said light-transmitting surface and calculating said quiescent drain-source current by subtracting said quiescent source current from said quiescent drain current.

38. The method of claim 35, further comprising:
sensing a quiescent source current from said source regions in dark conditions,
sensing a source current from said source regions during said illuminating, and
calculating said photo-induced drain-source current variation by subtracting from said source current said quiescent source current.

39. The method of any one of claims 32 to 38, wherein said pre-determined wavelengths are selected such that a plurality of different spectral components of said light can be determined from said output signals.

40. The method of claim 39, wherein said plurality of spectral components comprise a blue component, a green component and a red component.

41. The method of claim 40, wherein said blue component covers wavelengths below about 500 nm, said green component covers wavelengths from about 500 to about 600 nm, said red component covers wavelengths above about 600 nm.